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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/801,431

03/16/2004

David Alan Johnson

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3091

7590

02/13/2006

David A. Johnson
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EXAMINER

FENTY, JESSE A

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.		Applicant(s)	
	10/801,431		JOHNSON ET AL.	
	Examiner		Art Unit	
	Jesse A. Fenty		2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some * c) ☐ None of:
 - 1. ☐ Certified copies of the priority documents have been received.
 - 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>06/09/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 1-8 are objected to because of the following informalities: In re claim 1, the limitation, "with significant topography reduction compared to the traditional composite dielectric structure" is vague and indefinite because there is no traditional composite dielectric structure. Without more, such a statement is vague and indefinite and is not given patentable weight regarding the final structure of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The rejection of claims 4 and 5 under 35 U.S.C. 112, first paragraph, in the Non-Final Rejection mailed 03/22/05 is withdrawn. Applicant's admission that such layers are "known to those skilled in the art, and not relevant to the invention" is sufficient to render the limitations anticipated by the prior art regarding the final determination of patentability.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by
Deshpande et al. (US 2004/0242010 A1).

In re claim 1, Deshpande (esp. Fig. 3E) discloses a structure providing anneal cap/ion implant mask (68), and shallow trench isolation (70) features for III-V devices comprising a trench etched into the semiconductor, a combination anneal cap/CMP stop layer, and a dielectric trench fill layer, with significant topography reduction compared to the traditional dielectric structure.

In re claims 2, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs (section [0038]).

In re claims 3, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP (section [0038]).

In re claim 4, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs with over-layers of other semiconductors specific to the devices fabricated¹.

In re claim 5, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP with over-layers of other semiconductors specific to the devices fabricated².

¹ As described in sections [0069 - 0071], the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as a gate polysilicon layer, as is well known in the art.

² As described in sections [0069 - 0071], the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as a gate polysilicon layer, as is well known in the art.

In re claim 8, Deshpande discloses the device of claim 1, wherein said dielectric trench fill layer is silicon dioxide (section [0061]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deshpande et al. as applied to claim 1 above, and further in view of Ohta (US 2004/0126990 A1).

In re claim 6, Deshpande discloses the device of claim 1, but does not expressly disclose the silicon nitride layer being in the range of 100 to 3000 angstroms. Ohta discloses a silicon nitride liner having a thickness of 20 to 40 nm, which equates to 200 to 400 angstroms. It would have been obvious for one skilled in the art at the time of the invention to use a thicker liner layer as disclosed by Ohta for the device of Deshpande for the purpose, for example, of enhancing FET characteristics, such as increased drain current, by generating greater tensile stress in the silicon nitride layer (Ohta; sections [0032, 0045, 0056]).

In re claim 7, Deshpande discloses the device of claim 1,. Ohta discloses a silicon nitride liner having a thickness of 20 to 40 nm, which equates to 2 to 4 percent of the trench depth. Deshpande discloses the claimed invention wherein the trench depth

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is in the range of 1 μ m (1000nm), section [0047], but does not expressly disclose the silicon nitride layer having a thickness of 5 to 25 percent of the trench depth. It would have been obvious to one having ordinary skill in the art at the time the invention was made to increase the thickness of the nitride liner since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. To do so would improve the FET characteristics, such as drain current, as disclosed by Ohta (sections [0032, 0045, 0056]).

Response to Arguments

1. Applicant's arguments filed 06/06/05 have been fully considered but they are not persuasive.

a. First, applicant argues that Deshpande in Fig. 3E does "not illustrate the final structure formed in fabricating the device..." However, as noted in the Deshpande reference under the "Brief Description of the Drawings," Deshpande discloses that Fig. 3E is the final drawing of the first embodiment of the invention. This can also be seen from paragraph [0064] – [0065], where Deshpande stops describing the Fig. 3 embodiments, and begins to describe Fig. 4 and beyond.

b. Second, applicant asserts that there is an additional thermal oxidation process that much be performed for the device of Deshpande that will produce an additional layer not essential to the device of the instant application.

- i. To satisfy 35 USC 102, a prior art reference may consist of more components than a claimed invention, so long as the prior art contains all of the essential elements of the claimed invention in a consistent manner. For example, if a claim asserts a three-layer insulation stack of A/B/C, and the prior art teaches a four-layer stack of A/B/C/D, then the prior art duly anticipates the claim, even though there is an additional layer. Such is the case here. Applicant is asserting that the disclosure of Deshpande discloses more than is claimed. That fact is not a bar to the anticipation determination under 35 USC 102.
- ii. Second, applicant does not establish where in Deshpande this thermal oxidation layer is disclosed and the underlying structure differs from that claimed.
- c. Third, applicant argues that Deshpande is using his structure for a different use than the claimed invention. Specifically, that Deshpande is using the structure for the minimization of the bird's beak effect. Intended use descriptions do not make or break patentability determinations. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art. Therefore, if the prior art uses the disclosed device for a purpose not enunciated or contemplated by the applicant, such a distinction does not eliminate the prior art from anticipation or obviousness consideration.

- i. Additionally, the language of applicant, "a combination anneal cap/CMP stop layer" is intended use language that does not work to further define the claimed structure over the prior art. As claimed, applicant's structure comprises a III-V substrate, a trench liner layer, and a fill layer. The same is disclosed by Deshpande.
- d. Lastly, applicant argues that Deshpande does not disclose an anneal cap or that the thermal oxide layer grown from the semiconductor substrate is likely to be a poor anneal cap. Whether applicant characterizes the anneal cap of Deshpande as good or poor does not obviate the fact that Deshpande disclose an analogous structure to that of the claimed invention.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

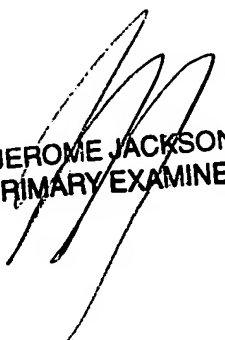
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815


JEROME JACKSON
PRIMARY EXAMINER